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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/583,744	06/20/2006	Nobuhiro Nishikawa	040894-7459	7122
9629 7590 10/17/2008 MORGAN LEWIS & BOCKIUS LLP 1111 PENNSYLVANIA AVENUE NW WASHINGTON, DC 20004				
EXAMINER SURYAWANSHI SURESH				
ART UNIT		PAPER NUMBER		
2115				
MAIL DATE		DELIVERY MODE		
10/17/2008		PAPER		

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/583,744

Applicant(s)

NISHIKAWA ET AL.

Examiner

SURESH K. SURYAWANSHI

Art Unit

2115

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 20 June 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 17 March 2006 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-893)
- 4) ☐ Interview Summary (PTO-413)
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____
- Paper No(s)/Mail Date 6/20/06

DETAILED ACTION

1. Claims 1-8 are presented for examination.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Nakane (US Patent 6,240,534).

4. As per claims 1 and 2, Nakane clearly discloses a monitoring circuit comprising a capacitor, charging means for charging the capacitor, discharging means for discharging the capacitor, voltage comparing means for comparing a certain reference voltage with a charging voltage of the capacitor, thereby generating a signal for resetting an operation of a monitoring object when the capacitor is charged to have a certain voltage or more, and source voltage deciding means for monitoring a source voltage of the monitoring object and resetting the operation of the monitoring object when the source voltage of the monitoring object is equal to or lower than a certain voltage [Abstract; Fig. 1, 7A and 7B; col. 4, lines 1-17; abnormality-monitoring circuit; col. 4, lines 34-36; comparator; col. 5, lines 25-31; col. 5, line 66 – col. 6, line

4; if source voltage is low, a reset signal RST outputted to the CPU; col. 9, lines 1-16; col. 11, lines 6-10; clearly there are two comparison reference voltages (V1 and V2) utilized where V1 is a low threshold voltage and V2 is a high threshold voltage].

5. As per claim 3, Nakane discloses that the source voltage deciding means is constituted by a comparator and the charging means is constituted by a current source [Fig. 1; col. 4, lines 1-17].

6. As per claim 4, Nakane discloses that the first discharging means is constituted by a current source and the second discharging means is constituted by an analog switch, and either or both of the first and second discharging means is/are operated to invert an output of the voltage comparing means, thereby resetting the monitoring object when the source voltage of the monitoring object is equal to or lower than a certain voltage [Fig. 1; col. 4, lines 1-17; col. 4, lines 34-36; col. 5, lines 25-31; col. 5, line 66 – col. 6, line 4; col. 9, lines 1-16; col. 11, lines 6-10].

7. As per claim 5, Nakane discloses that the first discharging means is constituted by a current source and the second discharging means is constituted by an N-type MOS transistor [Fig. 2].

8. As per claim 6, Nakane discloses that the voltage comparing means is constituted by a window comparator [Fig. 2].

9. As per claim 7, Nakane discloses that the voltage comparing means is constituted by a hysteresis comparator [col. 4, lines 63-67].

10. As per claim 8, Nakane discloses that the capacitor is provided on an outside of the semiconductor device [Fig. 1; capacitor is outside the resetting portion].

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to SURESH K. SURYAWANSHI whose telephone number is (571)272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Suresh K Suryawanshi/
Primary Examiner, Art Unit 2115